IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Kenneth A. Bandy, et al.	**Examiner:**	Lan Vinh
Serial No.:	10/604,087	**Art Unit:**	1765
Filed:	June 25, 2003	**Docket:**	BUR920020075US1 (16215)
For:	MULTI-RUN SELECTIVE PATTERN AND ETCH WAFER PROCESS	**Dated:**	June 17, 2005

Confirmation No. 1086

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION PURSUANT TO 37 C.F.R. §1.131

Sir:

We, KENNETH A. BANDY, VINCENT J. CARLOS, MARK D. LEVY, SARA L. LUCAS, TIMOTHY C. MILMORE, MATTHEW C. NICHOLLS, and JASON NOWAKOWSKI hereby declare that:

1. We are the co-inventors of the subject matter described and claimed in the above-identified patent application.

2. We conceived and reduced to practice the invention, which is disclosed and claimed in the present application, that is directed to a method for processing a semiconductor wafer including etching one or more first regions of a wafer according to a first set of variables, where a remaining portion of the wafer is prevented from being etched; and etching one or more other regions of the remaining portion of the wafer according to another set of etch variables, wherein one or more previously etched first regions and any remaining portion

of the wafer is prevented from being etched, in the United States, prior to August 8, 2002, which is the effective U.S. filing date of U.S. Patent Number 6,846,618 to Hsu, et al. (hereinafter "Hsu").

3. As evidence of the conception and reduction to practice of the method for processing a semiconductor wafer referred to in paragraph 2 prior to the effective U.S. filing date of Hsu, annexed hereto are Exhibits A and B. Exhibit A consists of a photocopy of the "Main Idea" section of IBM Invention Disclosure BUR8-2001-0375, which was created prior to August 8, 2002. Exhibit B is a photocopy of an electronic mail between one of the inventors and one legal counsel of IBM. Dates and names have been redacted in the preparation of the photocopies contained in the attached exhibit.

4. Specifically, Exhibit A is a photocopy of the "Main Idea" section of IBM Invention Disclosure BUR8-2001-0375 that recognized that there was a need for a multi-run wafer production method having a regional selective etch treatment that overcomes the limitations of the current process steps, and such a multi-run wafer production method improves yields and manufacturability via selectively etching predetermined regions of a semiconductor wafer throughout wafer production.

Moreover, included on Page 1 in Exhibit A is the description of a method for processing a semiconductor wafer that includes etching one or more first regions of a wafer according to a first set of variables, where a remaining portion of the wafer is prevented from being etched; and etching one or more other regions of the remaining portion of the wafer according to another set of etch variables, wherein one or more previously etched first regions and any remaining portion of the wafer is prevented from being etched.

Exhibit B further reveals a flow diagram of a multi-run selective pattern and etch wafer process, a flow diagram of a multi-part number multi-run selective pattern and

etch wafer process, and a pictorial representation (top view) of a wafer exhibiting line-stripping effects.

5. We do hereby declare that all statements made herein of our own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. section 1001, and that such willful false statements may jeopardize the validity or enforceability of the patent.

Respectfully submitted,

Dated: 6/13/05 — KENNETH A. BANDY

Dated: _____ — VINCENT J. CARLOS

Dated: _____ — MARK D. LEVY

Dated: _____ — SARA L. LUCAS

Dated: 6/16/05 — TIMOTHY C. MILMORE

Dated: 6/6/05 — MATTHEW C. NICHOLLS

Dated: 6/8/05 — JASON NOWAKOWSKI

etch wafer process, and a pictorial representation (top view) of a wafer exhibiting line-stripping effects.

5. We do hereby declare that all statements made herein of our own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. section 1001, and that such willful false statements may jeopardize the validity or enforceability of the patent.

Respectfully submitted,

Dated: _____ _____
KENNETH A. BANDY

Dated: June 6, 2005 _____
VINCENT J. CARLOS

Dated: June 6, 2005 _____
MARK D. LEVY

Dated: _____ _____
SARA L. LUCAS

Dated: June 13, 2005 _____ (formerly Lucas)
TIMOTHY C. MILMORE

Dated: _____ _____
MATTHEW C. NICHOLLS

Dated: _____ _____
JASON NOWAKOWSKI